Mingkai Miao

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Education

Hong Kong University of Science and Technology (Guangzhou) Aug. 2024 – Present
the 1st year PhD student in Microelectronics Thrust
- Supervised by **Prof. Hongce Zhang**

University of Illinois at Urbana-Champaign Jan. 2023 – May. 2024
Master student in Electrical and Computer Engineering
- GPA: 3.91/4.0
- Courses taken: Analog Circuit Design, IoT and Cognitive Computing, Computer Organization and Design, Computer Organization, System-On-Chip Design, Embedded System Verification, Parallel Computer Architecture.

University of Electronic Science and Technology of China Sep. 2017 – Sep. 2021
B.Eng. in Electronic and Information Engineering
- Engineering GPA: 3.898/4.0 for 77-credit
- Mathematics GPA: 4.0/4.0 for 18.5-credit
- Ranking top 20% with CGPA 3.72/4.0

Primary Project

FPGA-Optimized Parallelism in Deep Neural Networks Jan 2024 – May 2024
University of Illinois at Urbana-Champaign Champaign, US
- Implement the LeNet network for handwriting recognition tasks on the Xilinx Pynq Z2 Board from three aspects: Hardware, Model Architecture, and Software. In terms of Hardware, use High Level Synthesis to design the hardware accelerator. For Model Architecture, optimize using Pruning and Quantization. On the Software side, an Interrupt Handler is designed to achieve Function Level Parallelism (with Dataflow support at the Hardware level). Compared to the CPU platform on Pynq Z2, a final acceleration of **63.7x** is achieved.
- **Project Link:** https://github.com/tracymiao111/CS533-FinalProject

5 stage pipelining RISC-V processor design Aug 2023 – Dec 2023
University of Illinois at Urbana-Champaign Champaign, US
- Implemented the multicycle 5 stage pipelined RV32I processor
- Implemented one-cycle hit i-cache, L2 unified cache and fully parameterized mutli-level d-caches (PLRU replacement policy) with an eviction buffer
- Implemented RISC-V M Extension, simple hardware prefetching
- Achieved the **3rd place (33 groups)** in UIUC Computer Organization and Design RV32I Competition in December
- **Project Link:** https://github.com/tracymiao111/Pipelined-CPU-Design

Low dropout regulator design Apr 2023 – May 2023
University of Illinois at Urbana-Champaign Champaign, US
- Designed a low dropout regulator (LDO) used to generate supply voltage to sensitive analog circuits on Cadence Virtuoso
- Achieved specifications including Input/Output voltage, Load current, DC load/line regulation, etc
- **Project Link:** https://github.com/tracymiao111/LDO-Design

Bearing fault diagnosis project based on deep learning techniques Nov 2020 – May 2021
University of Electronic Science and Technology of China Chengdu, China
- Tested on the fault bearing data set from Case Western Reserve University
- Built ARCRNet (Attentive Residual Convolution Recurrent Network) model to train data and achieved 92%+ accuracy under -6dB noise condition

Honors and Awards

Winner of University's First-class Merit-based Scholarship Fall 2018 & 2019
University of Electronic Science and Technology of China

Skills

Languages: English (IELTS 7.0; GRE 329), Chinese (Native)
Programming: SystemVerilog, C++, Python
Document Creation: Latex, Markdown